APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/652,137	08/29/2003	Raymond B. Essick IV	CML00772D	1175

			EXAMINER -
33117	7590	03/14/2006	TRAN, DENISE

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ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/652,137	ESSICK ET AL.
	Examiner	Art Unit	
	Denise Tran	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *19 December 2005*.

2a) ☒ This action is **FINAL**.   2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-23* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-23* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *29 August 2003* is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 are presented for examination.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5, 9-10, 15-17, and 21-22 are rejected under 35 U.S.C. 102(b) as being

anticipated by Watkins, U.S. Patent No. 5,937,436.

As per claim 1, Watkins shows the use of an address translation filter for filtering

a signal on a system bus coupled between a core processor and an external memory

unit (e.g., fig. 2A, system bus 230, 270, fig. 3, 320 coupled between a CPU 210 and

main memory 220 which is external from the CPU), the address translation filter

comprising:

a first interface operable to connect to the system bus and receive a virtual

memory address from an external device connected to the system bus (i.e., interface

between ATM device and el. 260 or ATU 450 wherein bus 320 is a bus of the system)

(e.g. figures 2a, 3, 4);

a second interface operable to connect to the system bus and transmit a physical

memory address to the external memory unit (i.e., interface between each device

connected to the system bus or I/O bus) (e.g. figure 2a and col. 5., lines 54-64; col. 3,

lines 65 to col. 4, lines 35); and

an address translation unit, external to the core processor and coupled between

the first and second interfaces (e.g., fig. 3, el. 260 or ATU 450, external to the CPU 210

and coupled between system bus interface and ATM interface), operable to determine

the physical memory address from the virtual memory address (e.g. figure 2a and col. 5,

lines 54-64).

As per claim 15, Watkins shows a method of memory address translation in a

bus coupled between a core processor and the external memory unit (e.g., fig. 2A,

system bus 230, 270, fig. 3, 320 coupled between a CPU 210 and main memory 220

which is external from the CPU), the method comprising: receiving a first bus signal

from a device via the bus (i.e., interface between each device connected to the system

bus or I/O bus) (e.g. figure 2a; col. 6, lines 45-65); translating a virtual memory address

specified by the first bus signal to a physical memory address in an address translation

filter (e.g. figure 2a and col. 5, lines 54-64; col. 6, lines 3-10; lines 45-65); and

transmitting a second bus signal via the bus to the external memory unit in accordance

with the physical memory address (i.e., interface between each device connected to the

system bus or I/O bus) (e.g. figure 2a; col. 6, lines 45-65; col. 5., lines 54-64; col. 3,

lines 65 to col. 4, lines 35).

As per claims 2 and 16, Watkins shows the use of the address translation unit

includes a lookup table indexed by virtual addresses and selecting a physical memory

address from the table (e.g. col. 6, lines 1-15 and col. 7, lines 45-55).

As per claim 3, Watkins shows the use of an address translation filter in

accordance with claim 2, wherein the lookup table is indexed by the most significant portion of a virtual address (i.e., because the entire virtual address is used for lookup, the most significant portion is also used) (e.g. col. 6, lines 1-15).

As per claim 4, Watkins shows the use of an address translation filter in accordance with claim 1, wherein the address translation unit comprises a translation lookaside buffer (e.g. col. 1, lines 50-55 and col. 6, lines 1-15).

As per claims 5 and 17, Watkins shows the use of a refresh logic unit operable to refresh the translation lookaside buffer when the virtual memory address is not matched by an entry in the translation lookaside buffer (e.g. col. 6, lines 15-65).

As per claim 9, Watkins shows the use of a digital processing system, comprising: a core processor (e.g. figure 2a, elements 240 or 210); an external memory unit (e.g. figure 2a, element 220); an external processing device (e.g. figure 2a, element 260); an address translation filter (e.g. col. 5, lines 54-64); and a system bus linking the core processor, the external memory and the address translation filter to each other and linking the external processing device to the address translation filter (e.g. figure 2a, element 230), wherein the address translation unit is operable to translate a virtual memory address received via the system bus from the external processing device into a physical memory address transmitted via the system bus to the external memory unit (e.g. figure 2a and col. 5, lines 54-64).

As per claim 10, Watkins shows wherein the address translation filter comprises:

a translation lookaside buffer; and a refresh logic unit operable to refresh the translation

lookaside buffer when the virtual memory address is not matched by an entry in the

translation lookaside buffer (e.g. col. 1, lines 50-55 and col. 6, lines 1-15 and col. 6,

lines 15-65).

As per claim 21, Watkins teaches the use of the second bus signal is transmitted

to the external memory unit (e.g. figure 2a and col. 5, lines 54-64).

As per claim 22, Watkins teaches the use the first bus signal is received from a

processing device (e.g. figure 2a and col. 5, lines 54-64).

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

5.   Claims 7, 14, 20 and 23 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Watkins, U.S. Patent No. 5,937,436.

As per claims 7 and 20, Watkins does not show the use of input clock signals

and output clock signals wherein the output clock signal is paused while the TLB is

being refreshed. "Official Notice" is taken that both the concept and advantages of

providing for output clock signal is paused while the TLB is being refreshed is well

known and expected in the art. It would have been obvious to one of ordinary skill in

the art to include output clock signal is paused while the TLB is being refreshed to

Watkins because it would provide for a reduction in power consumption.

As per claim 14, Watkins does not show the use of the bus being AMBA or AHB.

"Official Notice" is taken that both the concept and advantages of providing for an AMBA

or AHB bus is well known and expected in the art. It would have been obvious to one of

ordinary skill in the art to include either an AMBA or AHB bus to Watkins because it

would provide for compatibility between existing bus architectures and ability to handle

robust bus protocols.

As per claim 23, Watkins does not specifically show the use of transferring code

from a core processor to the processing device; and transferring an initial memory map

from the core processor to the address translation filter. "Official Notice" is taken that

both the concept and advantages of including transferring code from a core processor

to the processing device; and transferring an initial memory map from the core

processor to the address translation filter is well known and expected in the art. It would

have been obvious to one of ordinary skill in the art to include transferring code from a

core processor to the processing device; and transferring an initial memory map from

the core processor to the address translation filter to Watkins would provide for updating

or upgrading the software contained in the NIC and provide for the initial assignment of

virtual and physical addresses to the NIC.

6.   Claims 6, 8, 11-13, and 18-19 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Watkins, U.S. Patent No. 5,937,436 in view of McGrath, U.S. Patent

No. 6,671,791.

As per claims 6, 11, 12, 18 and 19, Watkins does not specifically show the use of

an output control link responsive to the refresh logic unit and operable to signal the core

processor when the translation lookaside buffer is to be refreshed and having the core

load the information into the translation buffers. McGrath shows the use of an output

control link responsive to the refresh logic unit and operable to signal a core processor

when the translation lookaside buffer is to be refreshed and having the core load the

information into the translation buffers (e.g. col. 18, lines 48-65). It would have been

obvious to one of ordinary skill in the art at the time the invention was made to combine

McGrath with Watkins because it would provide for reduction in circuitry and complexity

but not having additional hardware perform the load of the missed translation.

As per claim 8, Watkins does not specifically show the use of the virtual and

physical memory addresses have the same width. McGrath shows the use of the

virtual and physical memory addresses have the same width. It would have been

obvious to one of ordinary skill in the art at the time the invention was made to combine

McGrath with Watkins because it would provide for a reduction in the complexity of the

system by removing the need to translate between the two sizes.

As per claim 13, Watkins does not show the use of the TLB is refreshed via the system bus. McGrath shows the processor performing the refresh (e.g. col. 18, lines 48-65). Therefore the combined system would have one of the CPUs 210 sending the translation to the ATU to be stored. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine McGrath with Watkins because it would provide for reduction in circuitry and complexity but not having additional hardware perform the load of the missed translation.

7.   Applicant's arguments filed 12/19/05 have been fully considered but they are not persuasive.

8.   In the remarks, the applicant's argued that the network interface circuit only has one interface to the bus 270 and the I/O bus 270 does not couple between a core processor and an external memory unit as recited in claim 1.

The examiner disagreed with the applicant' argument because the Watkins teaches the system bus (fig. 2a, els. 230, 270, and fig. 3, el. 320) coupled between a core processor (fig. 2A. CPU210 and main memory 220) and the address translation unit or network interface circuit having more than one interfaces (e.g., figs. 3, 4, el. 260 or ATU 450, external to the CPU 210 and coupled between system bus interface and ATM interface). Also. Fig. 4, show an interface between bus 270 and the address translation e.g., fig. 4, el. 400 or a connection between el. 400 to bus 270)

9.   In the remarks, the applicant argued that in claim 1, the first and second

interfaces are interfaces with the same system bus.

The examiner disagreed with the applicant's argument because el. 230 and el.

270 are part of the system bus structure.

10.   In the remarks the applicant argued that Watkins does not teach a filter on the

system bus.

The examiner disagreed with the applicant's arguments, Watkins, col. 5, lines 55-

65 shows the address translation unit to block (i.e., bypass) some of the virtual address

to the I/O MMU 250 via the system bus (fig. 2a, els. 230, 270, and fig. 3, el. 320).

Therefore, Watkins teaches the filter on the system bus.

11.   In the remarks the applicant argued that Watkins does not teaches the address

translation unit receiving a bus signal from the bus, translating a virtual memory

address specified by the bus signal to a physical memory address in an address

translation filter, and then transmitting a bus signal to the bus in accordance with the

physical memory address.

The examiner disagreed with the applicant's arguments, Watkins shows

receiving a first bus signal from a device via the bus (i.e., interface between each device

connected to the system bus or I/O bus) (e.g. figure 2a; col. 6, lines 45-65); translating a

virtual memory address specified by the first bus signal to a physical memory address in

an address translation filter (e.g. figure 2a and col. 5, lines 54-64; col. 6, lines 3-10; lines

45-65); and transmitting a second bus signal via the bus to the external memory unit in

accordance with the physical memory address (i.e., interface between each device

connected to the system bus or I/O bus) (e.g. figure 2a; col. 6, lines 45-65; col. 5., lines

54-64; col. 3, lines 65 to col. 4, lines 35).

12.   In the remarks, the applicant's argued that Watkins provide nothing to motivate

one of ordinary skill in the art to consider a bus filter and it would not be obvious for one

of ordinary skill in the art for the address translation filter to both received and transmit a

system lock signal since Watkins does not disclosed the same protocol or operating on

a single bus.

In response to applicant's argument that the references fail to show certain

features of applicant's invention, it is noted that the features upon which applicant relies

(i.e., same protocol) are not recited in the rejected claim(s). Although the claims are

interpreted in light of the specification, limitations from the specification are not read into

the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In further discussion, according to the current specification, fig 2, teaches the bus

filter 118 operating on more than one bus. Therefore, Watkins provide one of ordinary

skill in the art to consider a bus filter and it would be obvious for one of ordinary skill in

the art for the address translation filter to both received and transmit a system lock

signal.

13.   In the remarks, the applicant argued that McGrath does not teach signaling

between a core processor and an external address translation filter.

In response to applicant's arguments against the references individually, one

cannot show nonobviousness by attacking references individually where the rejections

are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208

USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir.

1986). In this case, the combination of Watkins and McGrath teaches signaling

between a core processor and an external address translation filter. In particular,

Watkins teaches Watkins shows a bus coupled between a core processor and the

external memory unit (e.g., fig. 2A, system bus 230, 270, fig. 3, 320 coupled between a

CPU 210 and main memory 220 which is external from the CPU), translating a virtual

memory address specified by the first bus signal to a physical memory address in an

address translation filter (e.g. figure 2a and col. 5, lines 54-64; col. 6, lines 3-10; lines

45-65); and transmitting a second bus signal via the bus to the external memory unit in

accordance with the physical memory address (i.e., interface between each device

connected to the system bus or I/O bus) (e.g. figure 2a; col. 6, lines 45-65; col. 5., lines

54-64; col. 3, lines 65 to col. 4, lines 35).

14.   In the remarks, the applicant's argued that Watkins and McGrath fail to teach or

render obvious the citations of claims 6, 8, 11-13, and 18-19.

The examiner, disagreed with the applicant's argument, the combination

Watkins and McGrath does teach and render obvious the citations of claims 6, 8, 11-13,

and 18-19. In particular, as per claims 6, 11, 12, 18 and 19, Watkins does not

specifically show the use of an output control link responsive to the refresh logic unit

and operable to signal the core processor when the translation lookaside buffer is to be

refreshed and having the core load the information into the translation buffers. McGrath

shows the use of an output control link responsive to the refresh logic unit and operable

to signal a core processor when the translation lookaside buffer is to be refreshed and

having the core load the information into the translation buffers (e.g. col. 18, lines 48-

65). It would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine McGrath with Watkins because it would provide for

reduction in circuitry and complexity but not having additional hardware perform the load

of the missed translation.

As per claim 8, Watkins does not specifically show the use of the virtual and

physical memory addresses have the same width. McGrath shows the use of the

virtual and physical memory addresses have the same width. It would have been

obvious to one of ordinary skill in the art at the time the invention was made to combine

McGrath with Watkins because it would provide for a reduction in the complexity of the

system by removing the need to translate between the two sizes.

As per claim 13, Watkins does not show the use of the TLB is refreshed via the

system bus. McGrath shows the processor performing the refresh (e.g. col. 18, lines

48-65). Therefore the combined system would have one of the CPUs 210 sending the

translation to the ATU to be stored. It would have been obvious to one of ordinary skill

in the art at the time the invention was made to combine McGrath with Watkins because

it would provide for reduction in circuitry and complexity but not having additional

hardware perform the load of the missed translation.

15.   Applicant has failed to seasonably challenge the examiner's Official Notices in

the previous office action, those limitations are now considered as prior art. MPEP

2144.03.

16.   Applicant's amendment necessitated the new ground(s) of rejection presented in

this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37

CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the date of this final action.

17.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Denise Tran whose telephone number is (571) 272-

4189. The examiner can normally be reached on Monday, Thursday, and Friday from

9:00 a.m. to 5:30 p.m..

        If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Matt Kim, can be reached on (571) 272-4182. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

        Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Denise Tran

3/6/06